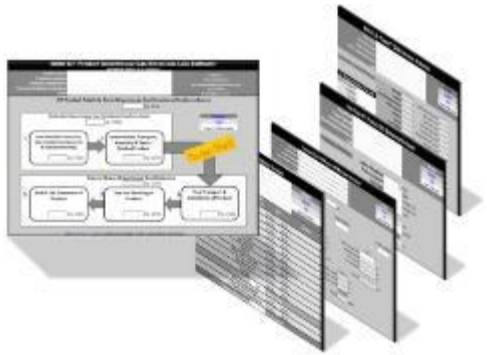
iNEMI Project Portfolio

iNEMI
March 12, 2021

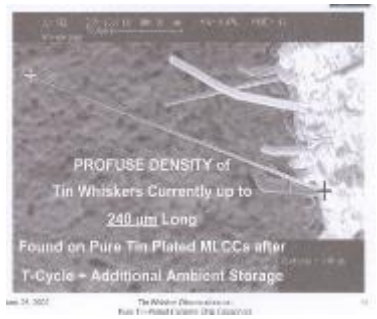
Advancing manufacturing technology

Profile of Successful iNEMI Projects

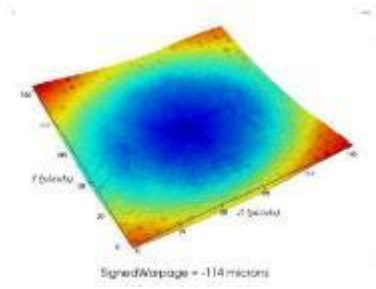
- Addresses industry knowledge gap
  - Common problem best addressed via industry collaboration
  - Often a pre-cursor to standards development
- Brings together a segment of the supply chain to provide an industry-wide response
- Direct alignment with member companies' commercial interests.
- iNEMI organizes and facilitates projects - typically 12-18 months long



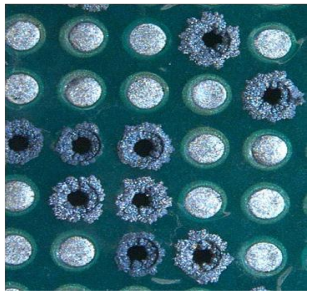
Eco-impact (LCA) Estimator



Tin Whisker Susceptibility



Warpage Characterization of Organic Packages



Creep Corrosion

Project Status
March 2021

15
ONGOING PROJECTS

1
PROJECTS FINISHED YTD

- Conformal Coating Evaluation for Improved Environmental Protection

2
PROJECTS STARTED YTD

- Data Management Best Practices for PCB Assembly
- Connector Reliability Test Recommendations Phase 3

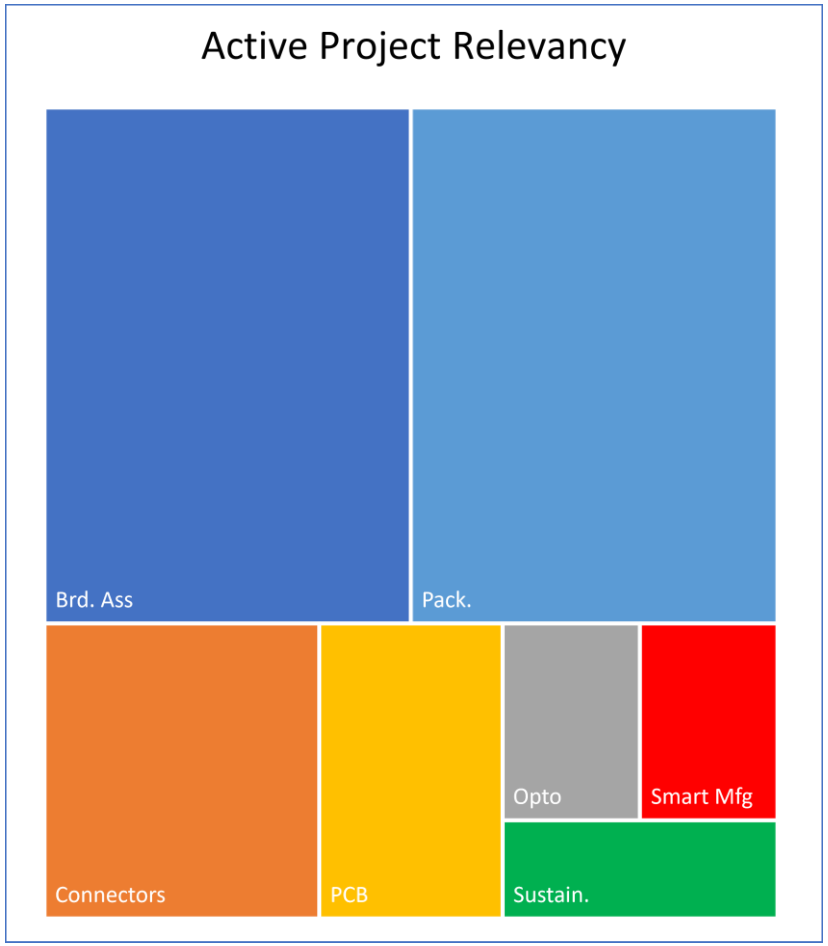
17
PROJECTS IN PIPELINE

- RDL Adhesion Strength Measurement in sign up
- 4 Initiatives for SOW review at TC this month

Collaborative Projects

15 Currently Active iNEMI Projects (March 2020)

Project Name	TIG
Eco-Impact Estimator Update Phase 3	SUST
Impact of Low CTE Mold Compound on Second Level Board Reliability Phase 2	BA
QFN Package Board Level Reliability Project	BA, PK
Wafer/Panel Level Substrate Fine Pitch Inspection/Metrology	PK
PCBA Materials for Harsh Environments Phase 2	BA, PCB
Package Warpage Prediction and Characterization	BA, PK
Data Management Best Practices for PCB Assembly Phase 1	SM, BA
Backend Commonality Advanced Packaging: Large Form Factor	SM, PK
5G/mmWave Materials Assessment and Characterization: Phase 1	PK, PCB
Best Practices & Guidelines for Use of Expanded Beam Connectors in Data Center Apps	OPTO,CONN
Characterization of 3rd Generation High Reliability Pb-Free Solder Alloys	BA
BiSn Based Low Temperature Soldering Process and Reliability	BA
1st level Interconnect Voiding Characterization	PK
High Density Interconnect Socket Warpage Prediction and Characterization	BA, CONN, PK
Connector Reliability Test Recommendations Phase 3	CONN



Project plans, results and presentations available at: https://community.inemi.org/projects_all

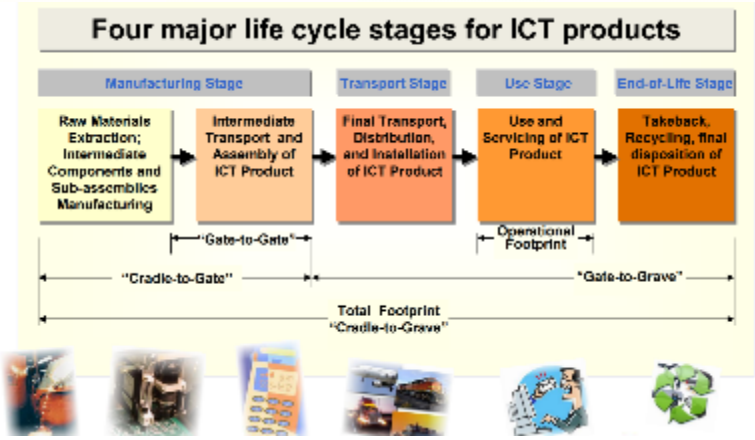
Eco-Impact Estimator, Phase 3
Sustainable Electronics

Motivation:

- Full featured LCA burdensome and not necessary for many applications Increasing need for eco-impact transparency and decision support

Objective:

- Develop an LCA-based estimator tool for assessing selected eco impacts of key electronic components
- Improve the component algorithms and methods for estimating the eco-impact of ICT products



Strategy/Approach:

- Leverage prior eco-impact estimator development in a now hosted environment
- Update life cycle eco impact data for key component categories – PWBs, ICs, cables, mechanical parts
- Expand product scope

Longer Term:

- Expanding eco-impact to additional aspects, e.g. water resource depletion
- Allow for broader access to online database promoting industry adoption
- Integration with other tools to provide a more transparent and holistic view of sustainability impacts

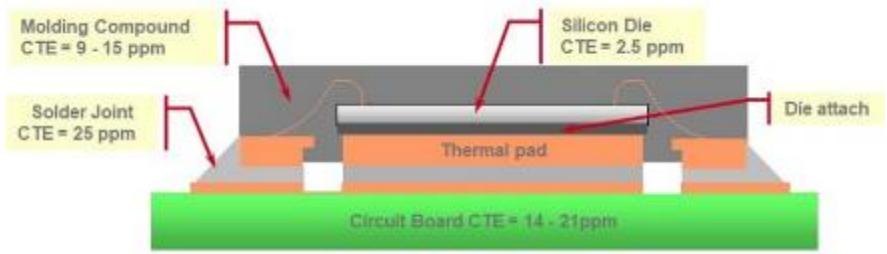
Status:

- Chaired by Nokia
- Paper presented EGG2020
- 3 Lifecycle stages in final update and debug (Transport, Use, End of Life)
- Projected Completion in April
- End-of-project report out April 27th
- Contact: Mark Schaffer (marks@inemi.org)

Impact of Low CTE Mold Compound on 2nd level Solder Joint Reliability – Phase 2

Motivation:

- Need to develop the data required to test the hypothesis that lowering the CTE value of the mold compound will impact BLR for various packages.



Objective:

- To increase the understanding of the relationship between the 2nd level solder joint reliability, the mold compound CTE and the component type, termination configuration and dimensions by studying the reliability performance of different package types with mold compounds of different CTE values
- To develop recommendations for minimum mold compound CTE to achieve the application dependent required reliability under specified test/operating conditions

Strategy/Approach:

- Design and assemble test vehicles with packages with mold compounds of different CTE values.
- Conduct thermal cycling and thermal shock testing on test vehicles

Longer Term:

- Leverage results to refine models in this area.
- Extend to other package configurations.

Status:

- Chaired by Nokia
- Completed CTE measurement on assemblies
- Completed Temperature Cycling to failure
- Investigating using data for model development
- Final report out Q2 2021
- Contact: gomalley@inemi.org

QFN Package Board Level Reliability
Board Assembly

Motivation:

- Published QFN thermal cycling data are lacking for characterizing longer product lifetimes, in more aggressive use environments, particularly using thicker printed circuit boards typical of higher reliability applications.
- Failure due to solder thermal fatigue is a principal concern due to the inherently high CTE mismatch, low solder standoff, and non-compliant peripheral interconnects of the QFN package.

Objective:

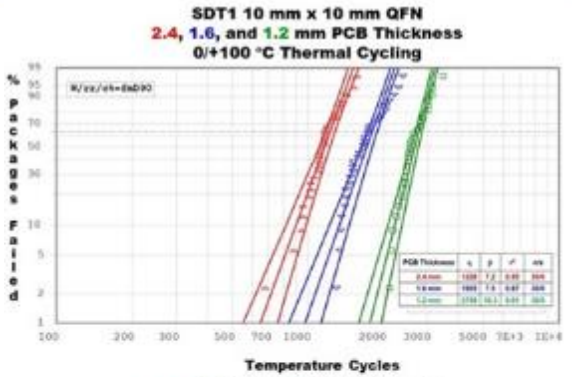
- Develop QFN BLR data as a function of three printed circuit board thicknesses and two different thermal cycles profiles. This will provide guidance for translating data from one board thickness or one temperature cycle to another.

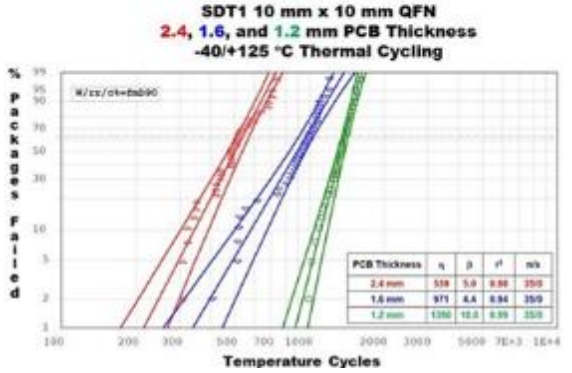
Strategy/Approach:

- Design and assemble variety of test vehicles with QFN packages.
- Conduct thermal cycling and thermal shock testing under varying conditions on test vehicles
- Verify failure modes

Longer Term:

- Leverage results to refine models in this area.





Status:

- Chaired by Nokia
- Test vehicles designed and assembled
- Thermal shock and thermal cycling testing conducted.
- Published paper at SMTAI in 2018
- Member presentation April 2019
- Final report out Q2 2021
- Contact: gomalley@inemi.org

Wafer/Panel Level Fine Pitch Substrate Inspection/ Metrology, phase 3
Packaging

Motivation:

- With the deployment of finer pitch substrate features in advanced packaging (SiP, 2.5D etc), there is a need to identify and characterize the capabilities of inspection technologies that can enable faster process development and higher yield in volume production. Continue from phase 2 to expand the study using organic TV.

Objective:

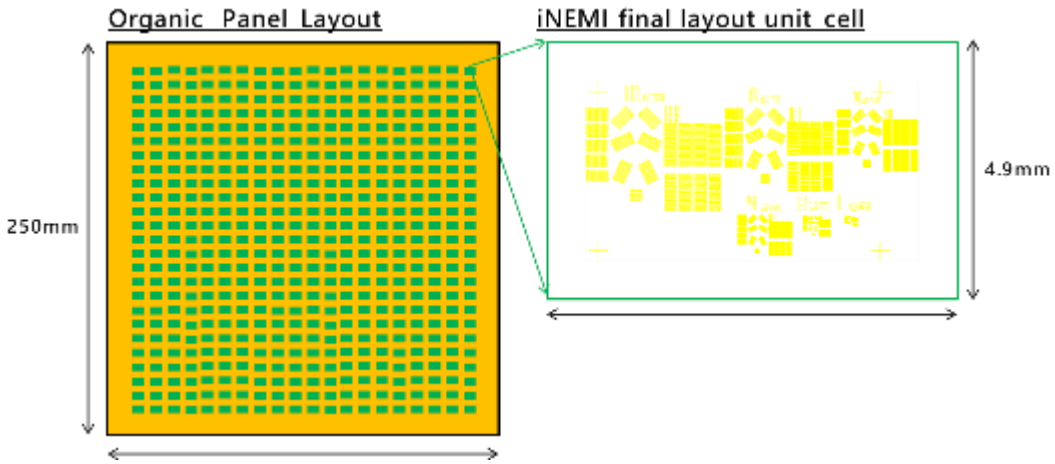
- Evaluate current inspection & measurement capabilities for fine pitch substrates that will be needed over the next 5 years.

Strategy/Approach:

- Fabricate Test Vehicle on organic substrate using the same TV designs with phase 2 project.
- Understand and quantify the automatic optical inspection (AOI) capability limitations for the fine pitch patterns and defects on TVs
- Compare with other metrologies such as SEM or OGP and identify the different capability results among the TV substrate.

Longer term:

- Analyze the measurement data and compare the data with AOI equipment type and other metrologies and TV substrate types.



Status:

- 8 member team, Chaired by IBM and Intel
- Started March, 2020
- Completed fabrication of Organic Panel TVs
- Completed measurement procedure documentation for AOI inspection partners
- Completed warpage measurement of cell and entire sub-panel
- Completed measurement of trace widths by CMM, X-sectioning and SEM measurement
- Samples at AOI inspection incl. trace width measurement, defects detection repeatability per each defect levels
- Contact:m.tsuriya@inemi.org

PCB & PCBA Material Characterization for Harsh Environment Project Phase 2

Motivation:

- PCBA modules can pass existing specifications but still experience field failures due to harsh environments. There is a need for all-encompassing testing procedures for PCBA materials in harsh environments

Objective:

- To develop a common test vehicle to accurately reflect typical DUT (device under test) modules, and to validate or develop relevant pass/fail criteria for PCB and PCB assembly materials in harsh environments

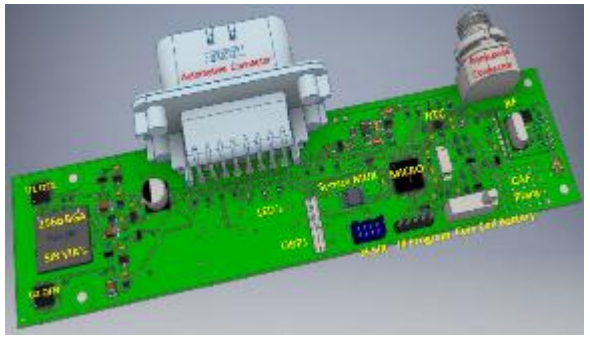
Strategy/Approach:

- Develop a methodology for cost effective materials pre-qualification (screening) for harsh environments. Enable OEMs to easily compare material datasheets from differing suppliers. Reduce costs and timescales in re-qualifying products for each OEM specification.

Longer term:

- Report to standard bodies

U41 Test vehicle



Status:

- Chaired by Foresite – 11 members
- Initial shock -40 to +125C & FEA undertaken on U41 TV
- Test vehicle (U41) re-design & in-situ testing capability being developed
- Parallel BGA TV for thermal shock v thermal cycling being planned
- Team planning next stage of thermal testing
- Assessing extended evaluation time scale or Phase 3
- Contact Steve.Payne@inemi.org

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Package Warpage Prediction and Characterization Project

Warpage Characterization and Management Program, Phase 5

Motivation:

- Dynamic warpage characterization of evolving electronic package types is critical for seamless board assembly and high yield.

Objective:

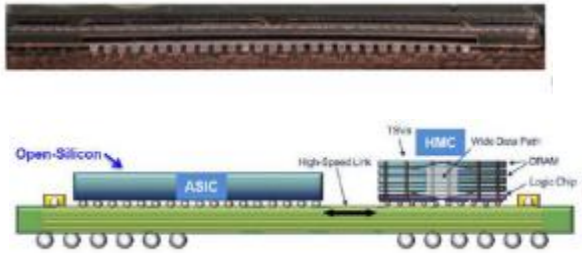
- Characterization of latest packaging technology warpage – what is realistic today and tomorrow
- Package warpage prediction – establish a reliable modelling framework to optimize package warpage simulation

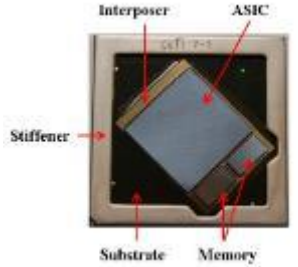
Strategy/Approach:

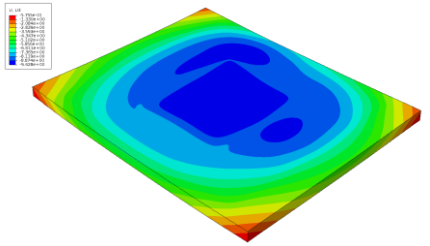
- Collect samples via donation from industry with a focus on advanced and large packages; team will measure and analyze the dynamic warpage and share results anonymously
- Conduct simulation and physical experiment to quantify how warpage evolve during the assembly (substrate or package), compare simulation with physical results to identify gaps
- Based on early phase's results, further investigate organic substrate-based packages, enhance material properties characterization (e.g. substrate raw material) to help us understand the impact of curing process on eventual package warpage.

Longer term:

- Improve model generation, material properties characterization, and simulation capabilities
- Provide opportunity for simulation software providers to validate or develop capabilities to meet the electronic packaging needs







Status:

- Chaired by Intel
- 9 Members Intel, Flex, CoreTech, Anasys, Shinko, Akrometrix, Insidix, Fraunhofer IZM. More welcomed
- Conducted preliminary simulation and comparing results, analyzing the gaps
- Characterizing raw material; TVs under warpage measurement
- Submited abstract to ICEP 2021
- Contact: Haley.Fu@inemi.org

Data Management Best Practices for PCB Assembly
Smart Manufacturing

Motivation:

- Diverse SMT equipment vendors with different software and operating systems of various vintages
- An automated method to collect, analyze and use machine/process data is a key enabler to the factory of the future

Objective:

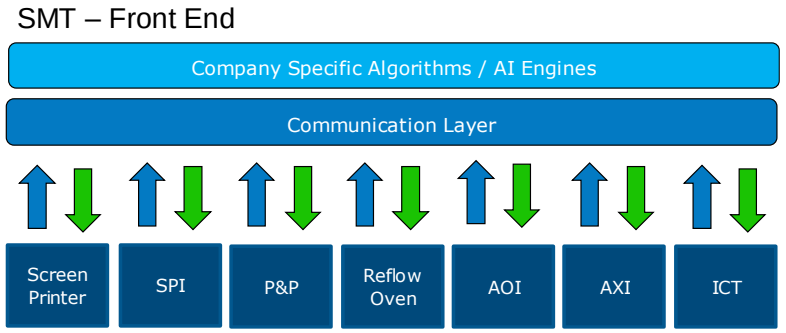
- Develop a generic reference data architecture and best practices to enable efficient implementation of Smart PCB assembly in a manufacturing environment where diverse supplier equipment is used

Strategy/Approach:

- Identify the common data sets required from/to machines and processes
- Define guidelines for data format, inputs/outputs, timing, frequency etc.
- Utilize an available industry standard for M2M communications
- Physical implementation to validate best practices and demonstrate the ability to improve process/machine performance

Benefits:

- Efficient implementation of Smart PCB assembly within an existing manufacturing footprint
- Automated machine/process control for improved line performance



Status

- Chaired by Cimetrix
- 6 Industry team participants: OEM/IDM, software, inspection and metrology
- Key task teams have formed – one working on use case (pick and place) and another working on data sets/needs across Smart Manufacturing
- Meeting weekly, open to additional members
- Contact: marks@inemi.org

Back End Commonality for Advanced Packaging: Large Form Factor
Smart Manufacturing/Packaging

Motivation:

- Advanced Packaging and adoption of heterogeneous integration and system in package (SiP), drives the trend for larger packages, with unique challenges both in semiconductor assembly (chip to package), as well as PCB assembly (package to board)

Objective:

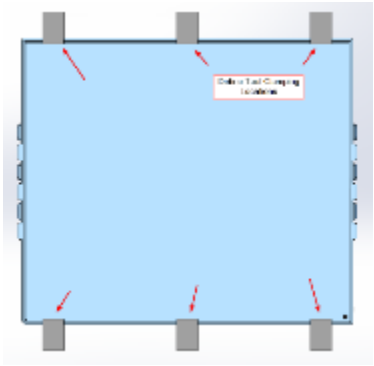
- Demonstrate and drive new requirements and guidelines for emerging packages for cost-effectiveness and operational efficiency

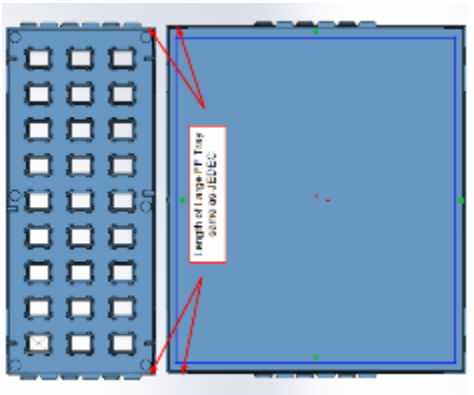
Strategy/Approach:

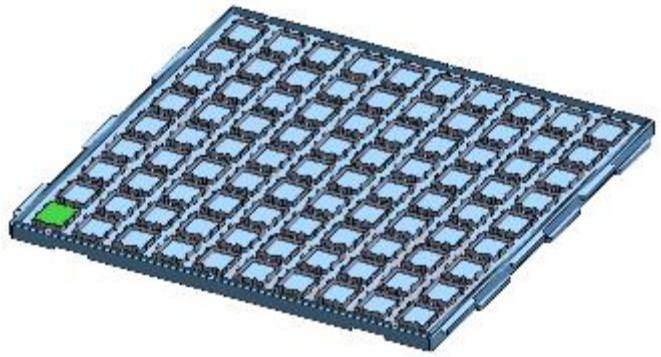
- Large media (JEDEC tray, carrier) Focus
- Identify common requirements
- Demonstrate Proof-of-concept
- Recommendation to standards organization(s)

Milestone:

- Phase I: Requirements
- Phase II: Proof of concept/Feasibility demo
- Phase III: Drive standards







Status:

- Project launched Nov'19,
- Chaired by Intel , 9 members
- Phase I Completed Mar 2020
- Proof of concept design underway
- Final design review completed
- Contact Urmi.Ray@inemi.org

5G/mmWave Materials Assessment and Characterization
Materials Challenges for 5G

Motivation:

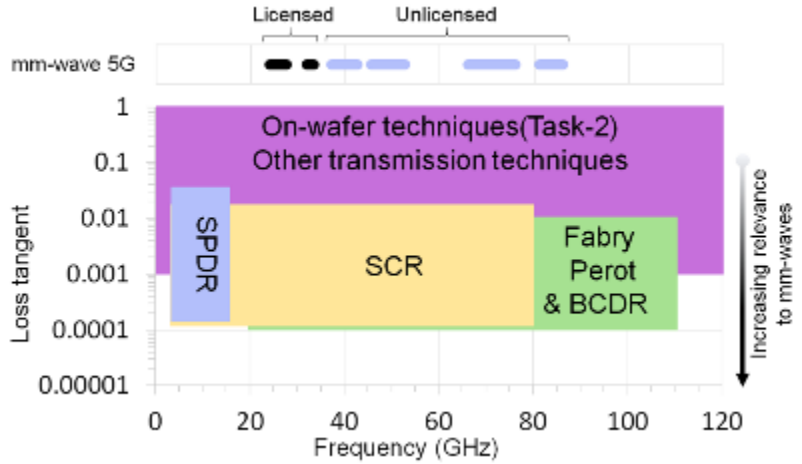
- 5G Solutions requires the ultra-low loss laminate materials
- The transmission loss or Df/Dk measurement methodology is still limited measuring under the use condition (up to 100GHz frequency)
- Many different test methods currently in the industry
- Benefit to the industry to have standardized measurement methods and the possible standard test coupon.

Objective:

- Characterize Ultra Low Loss laminate materials using the proposed Df/Dk measurement methodologies under the range of 30 – 100GHz and provide guideline of best practices to the industry

Strategy/Approach:

- Develop a guideline/best practices for standardized measurement/ test technique
- Develop a standardized method of Dk, Df measurement
- Propose "standard" test coupons for industry wide application (Phase 2



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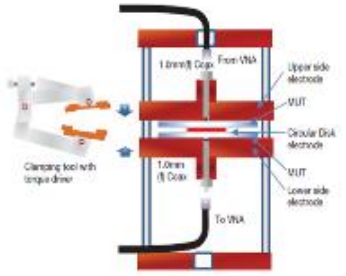


BCDR

Status:

- Chaired by Keysight and ITRI - 25 members
- Two reports on 5G current & emerging test methods issued
- Round robin reference standard measurement underway
- Hosting 5G webinar series, sessions at IPC APEX and IMAPS, paper at ICEP
- Contact: Urmi Ray

Best Practices and Guidelines for the Use of Expanded Beam Connectors in Data Center Applications

Motivation:

- Expanded beam connectors are less sensitive to contamination than physical connectors and promise cost savings due to reduced cleaning requirements and potentially higher reuse of connectors for data centers
- There are no standard cleaning methods or guidelines for effective cleaning processes for expanded beam connectors. These are required to enable the use of expanded beam connectors in the datacenter environment, as well as HPC and other applications

Objective:

- To investigate the impact of contamination on optical performance (IL, RL) of expanded beam connectors
- To develop recommendations for cleaning processes for single mode, and multi-mode expanded beam connectors
- To validate the potential operational and maintenance cost savings in the data centers due to reduced cleaning of expanded beam connectors

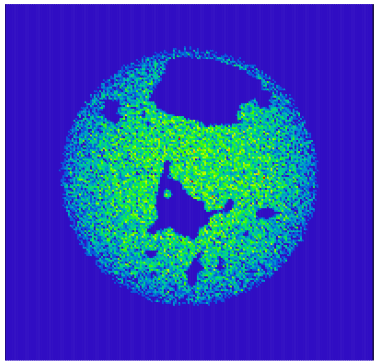
Strategy/Approach:

- Compare the performance of clean and contaminated expanded beam connectors
- Compare the optical performance of contaminated (without cleaning) expanded beam, air gap, and physical contact connectors
- Calculate potential maintenance cost savings in the data centers due to implementation of expanded beam connectors in comparison to physical connectors (cleaning time, materials etc).
- Compare different cleaning methods and processes for effective cleaning of multi-mode and single mode expanded beam connectors

Outputs:

- Report to industry on cost benefits opportunities for use of expanded beam connectors
- Present recommendations on cleaning processes and best practices to IEC and other standards bodies

Example



Simulated loss: 1.11dB

Calculated loss: 1.17dB

Measured loss: 1.70dB

Status:

- Project Started in Dec 2020
- Chaired by Senko with 10 members - more participation welcomed
- Cost model development started
- DoE being finalized by Team
- Wide range of containments and environment being considered
- Contact: Steve.Payne@inemi.org

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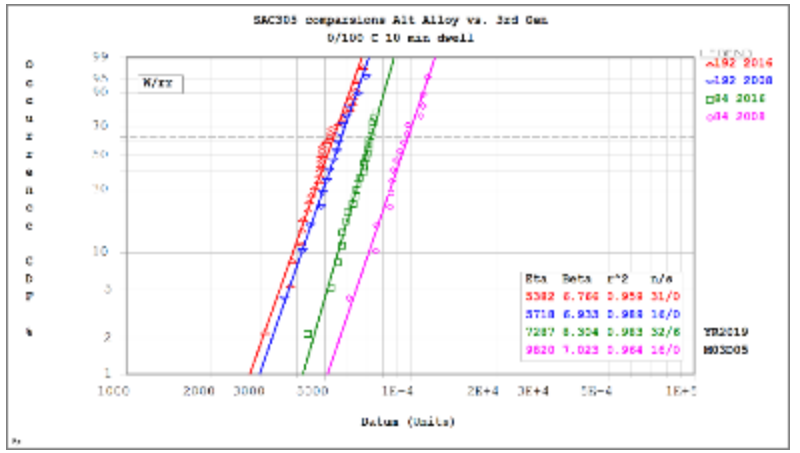
Characterization of 3rd Gen Pb-Free Alloys
Board Assembly

Motivation:

- Thermal fatigue data for new, third generation Pb-free alloys is needed, including a better understanding of the impact of additions of 4th and 5th element major alloying additions, as well as micro alloy additions, on performance.



Objective:

- Establish the correlation between microstructure and thermal fatigue performance

Strategy/Approach:

- Leverage test vehicle for thermal shock and cycling testing over different ranges
- Assemble and test of 10+ different solders alloys with different surface finishes and components
- Conduct detailed failure and microstructural analysis

Longer term:

- Extend studies on effect of longer dwell times and vibration
- Recommendations for test methods to the IPC to consider for standardization

Status:

- Chaired by Nokia, 12+ members
- Conducting thermal cycling with BGA and resistor test vehicles
- Planning additional testing including longer dwell times and thermal shock testing
- Working with Imperial college London on microstructure analysis
- Publications at SMTAI 2018, 2019 and 2020 and in SMTA Journal
- Contact gomalley@inemi.org

BiSn Based Low Temperature Soldering Process and Reliability
Board Assembly

Motivation:

- SMT Solder Joint Yield Losses are increasing due to the increased use of ultra-thin electronic packages and boards. Higher energy costs are driving ODMs to reduce power usage in manufacturing process

Objective:

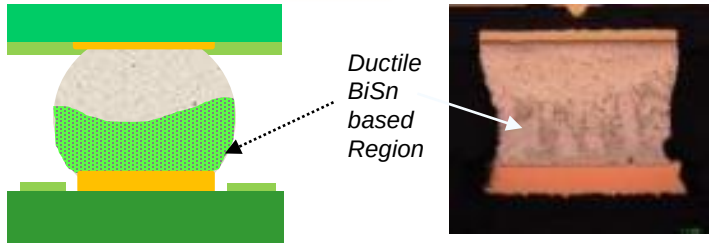
- To assess the surface mount process-ability and reliability of the solder joints formed when enhanced Bi-Sn based solder pastes are used for assembling electronic components on printed circuit boards

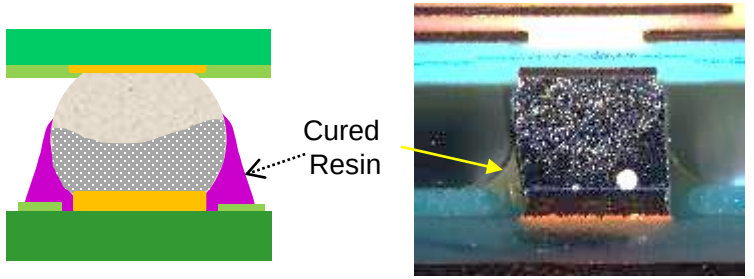
Strategy/Approach:

- Resin reinforced, and ductile Bi-Sn metallurgy solder paste are potential solution paths to mitigate risks of Bi-Sn brittle solder joints

Longer term:

- Accelerate the LTS material development and prepare technology for future application needs





Status:

- Chaired by Intel 20+ members
- Publications at SMTAI 2017, SMTA Pan Pac 2018, ICEP 2018 and SMTAI 2018, Pan Pac 2019, SMTAI 2019, SMTAI 2020
- Finished process development and originally planned Mech Shock Test and FA
- Conducting Thermal Cycling Test and extra Mech shock testing
- Contact Haley.Fu@inemi.org

1st Level Interconnect Voiding Characterization
Packaging

Motivation:

- The formation of small voids (micro voids) can occur in solder-based flip chip joints during the assembly process, but criticality of voids in 1st level interconnect e.g. flip chip bump, for performance and reliability is not well known.
- There are no guidelines or standards presently which define an acceptable percentage of voiding or how the percentage of voiding relates to the reliability of the assembly.

Objective:

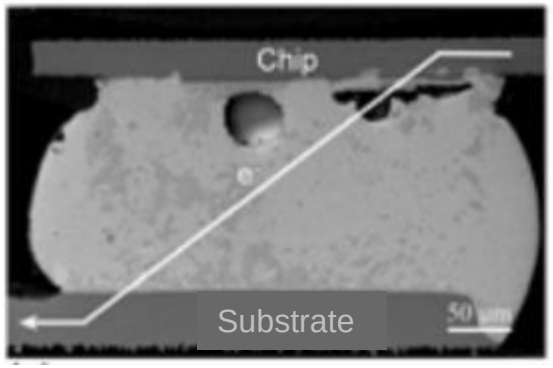
- Perform experimentation to understand the relationship between void and the joints reliability (electrical and mechanical)
- Strive to develop recommendations for the industry and standards bodies on the acceptable voiding characteristics for flip chip interconnects for the required packaging reliability.

Strategy/Approach:

- Study and determine the AOI inspection capability of micro-voids
- Characterize the flip chip assembly processes for micro-void formation in FC bumps
- Determine effect of micro voids on joint and device performance
- Study the relationship of void vs. electro-migration and TC/TS

Longer term:

- Recommend how to minimize voiding and how to inspect for it
- Develop guidelines that can be communicated to standards bodies



Status:

- Chaired by Intel, co-chaired by Shinko / Indium - 7 Members
- Started Feb, 2020.
- Completed phase 1 in Dec 2020
- Phase 1 report webinar on Feb 4, 2021
- Phase 2 underway
- study the voids impact to EM and TS/TC.
- Completed TV2 sample build (ball & paste bumps) for EM and TC/TS test
- Under void inspection. TS testing starting mid/Mar and TC/EM to start from May.
- Contact: m.tsuriya@inemi.org

High Density Interconnect Socket Warpage Prediction and Characterization

Warpage Characterization and Management Program, Phase 5

Motivation:

- Socket connectors are getting larger (>50x50mm) and density keep increasing which cause the challenges to socket warpage simulation and control

Objective:

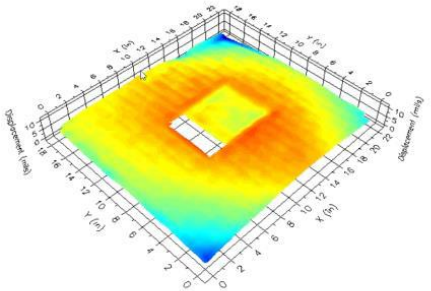
- Reduce the impact of socket warpage on PCBA yield and reliability.
- Characterize the impact of molding and design on large size socket warpage
- Develop socket warpage measurement guideline and prediction methods for large size socket

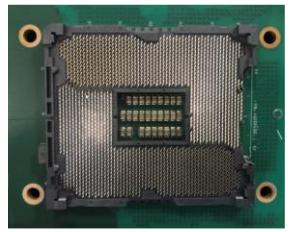
Strategy/Approach:

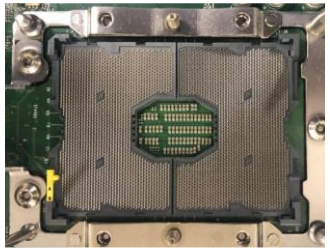
- Literature search on socket warpage related work from design, material, molding, SMT perspective, etc.
- Characterize the known sockets provided by donor and derive key learning on factors that affect the socket warpage
- Demonstrate the impact of socket design and process condition on socket warpage and study material properties sensitivity
- Explore adding weight to sockets for SMT process improvement

Longer term:

- More accurate and faster predictive simulation of socket warpage to improve time to market
- Establish best practices for socket warpage measurement via the collaboration with measurement tool suppliers







Status:

- Preliminary simulation results under review
- Selecting test vehicle & materials
- Preparing for TV build
- 10 Members: Intel, Flex, Lotes, CoreTech, Autodesk, Akrometrix, FCI-Amphenol, FIT, Insidix and Celanese
- More participation welcomed
- Contact: Haley.Fu@inemi.org

Connector Reliability Test Recommendations, Phase 3
Board Assembly / Connectors

Motivation:

- Address gaps in connector test coverage
- A standardized reliability test framework for evaluating electrical connectors across types and use conditions is needed

Objective:

- Define, develop and implement a test vehicle and test plan to verify the methodology proposed earlier work.

Strategy/Approach:

- Evaluate gaps in test coverage
- Develop and verify tests methods and/or test vehicle
- Develop recommended test conditions to reflect operational thermal shock

Longer term:

- Additional research needed on effects of dust concentration, particle size, temperature, and humidity on connector contact resistance
- Feed into ECIA and standards

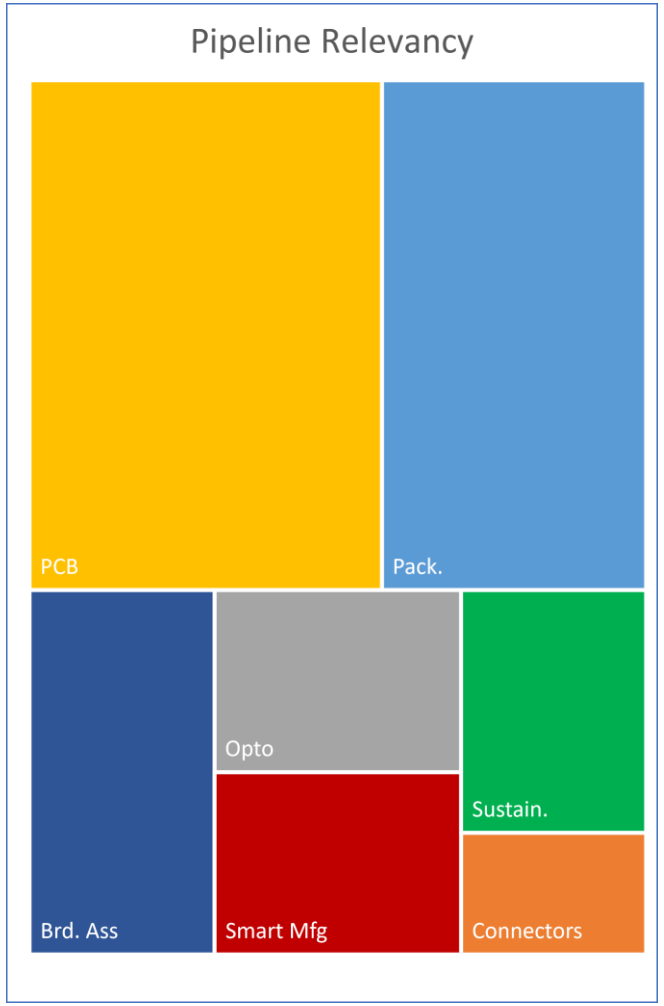
Test Order	Tests Required for All Connectors			Tests for Connectors w/ Precious Metal Finish	Tests for Connectors with Tin Plate (optional for <0.38 um Au plate)	Tests for Connectors with surface treatment or short wipe length (<0.127mm)	Tests for Connectors with more than 50 mate/unmate cycles
	1	2	3	4	5	6	7
1	Contact Resistance	Contact Resistance	Contact Resistance	Contact Resistance	Contact Resistance	Contact Resistance	Dielectric Withstanding Voltage
2	Mate/Unmate Cycles (preconditioning)	Mate/Unmate Cycles (preconditioning)	Mate/Unmate Cycles (preconditioning)	Thermal Shock	Thermal Shock	Mate/Unmate Cycles (preconditioning)	Contact Resistance
3	**Temperature Life**	Dust (preconditioning)	Temperature Life (preconditioning)	Mate/Unmate Cycles (preconditioning)	Mate/Unmate Cycles (preconditioning)	**Dust**	Mate/Unmate Cycles
4	Contact Resistance	Thermal Shock	Dust (preconditioning)	Temperature Life (preconditioning)	Temperature Life (preconditioning)	Contact Resistance	Contact Resistance
5	Reseating (mate/unmate)	Contact Resistance	**Vibration**	Contact Resistance	Contact Resistance	Thermal Cycling (disturbance)	Dielectric Withstanding Voltage
6	Contact Resistance	**Temp/Humidity Cycling**	**Shock**	**Mixed Flowing Gas**	**Thermal Cycling**	Contact Resistance	
7		Contact Resistance	Contact Resistance	Contact Resistance	Contact Resistance	Reseating (mate/unmate)	
8		Reseating (mate/unmate)		Thermal Cycling (disturbance)	Reseating (mate/unmate)	Contact Resistance	
9		Contact Resistance		Contact Resistance	Contact Resistance		
10				Reseating (mate/unmate)			
11				Contact Resistance			

Status:

- Chaired by Amphenol
- 5 companies Joined; open to more
- Team focusing on environmental conditions of G2.0 and G2.1 from EIA-364
- Team investigating Level 4 components to test while also considering adding USB-C to list of components
- Contact: Marks@inemi.org

Project Pipeline
Active and Anticipated (march)

Project Name	TIG	Stage
RDL Adhesion Strength Measurement	PK	Launch
Reliability & Loss Properties of Copper Foils for 5G Applications	PCB, PK	Planning
PIC Chip & Micro Optics Demonstrator for Edge pluggable free space connector	OPTO,CONN	Planning
Eco-Design for a Circular Economy -- Learning Series	SUST	Planning
Conformal Coating Phase 2	BA	Planning
Electromigration in Low Temperature Solder at Board level	BA, PK, PCB	Concept
PCB Fiberglass Cloth Characterization for CAF Failure Mitigation	PCB	Concept
Reliability Testing of Hybrid PCB for RF applications	PCB	Concept
Smart (AOI) Inspection: Capabilities & Gaps/Opportunities	BA, SM	Concept
Extended Reliability Assessment for Electronic Components	SUST	Definition
5G Test Methodology Challenges	PK, PCB	Concept
Embedded Components - Simulation/Modelling of thermal & elec performance	PCB, PK	TIG
Smart Manufacturing - Data Security	SM	TIG
Low Temp 1st Level Interconnect Challenges	PK	TIG
Advanced Packaging Test Methodology Optimization	PK	TIG
Pad Cratering Mitigation	PCB	TIG
PCB Level Interconnect for Co-Packaged Optics Challenges	PCB, OPTO	TIG



Project Development: Concept → Definition → Planning → Launch → Execute

RDL Adhesion Strength Measurement
Packaging

Motivation:

- RDL adhesion for advanced substrate, FO-WLP and PLP is critical for packaging quality. Poor adhesion strength causes circuit patterning quality and package reliability issues. Exposure of the RLD to the manufacturing process may degrade the adhesion between the RDL and other materials such as encapsulant, insulation, die, carrier wafer, substrate or panel.
- There is no global standard available to measure narrow RDL adhesion strength. The only available measurement standard (IPC) is for wider Cu trace adhesion to printed circuit boards.

Objective:

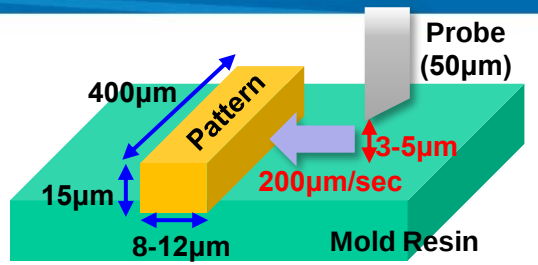
- Evaluate adhesion strength measurement methodologies and characterize the RDL mechanical performances.
- Establish the potential common requirements for key material properties so that packaging companies and users have identical qualification requirements.

Strategy/Approach:

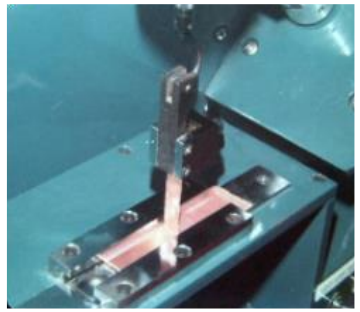
- Phase 1 - Evaluate the applicable adhesion strength measurement methodologies, validate the selected methodologies and develop the experimental guidelines.
- Phase 2 - Validate the test method(s) for characterizing the RDL by experiment.
- Generate lifetime data from accelerated tests and conduct failure analysis

Longer Term:

- Provide guidelines for narrow trace/RDL adhesion strength measurement and recommendations to a standard body for a global standardization test method(s).



Pattern Shear Strength Test Method



Status:

- Chaired by Intel and Unimicron
- Call for Participation webinar on Mar.3, 2021
- Project in Launch / Sign Up
- Open to new participants
- Contact Masahiro Tsuriya m.tsuriya@inemi.org

Reliability & Loss Properties of Copper Foils for 5G Applications

PCB / 5G

Motivation:

- Copper foil manufacturers apply treatments to copper foil and PCB fabricators treat copper surfaces to improve adhesion to resin systems. This treatment is often essential for PCBs to survive thermal shock but can have a detrimental effect to signal loss for high frequency / 5G applications which require very low-profile copper foil and low-loss resin systems for electrical performance.

Objective:

- To characterize various copper surface treatments to mitigate signal loss while maintaining good adhesion and, hence, durability of the PCB.

Strategy/Approach:

- Determine signal loss characterization for various surface topology & profilometry results for signal frequencies used in 5G applications.
- Determine and characterize copper to dielectric bond strength methodology for various copper foil thicknesses and types.

Longer term:

- Publish guidelines.

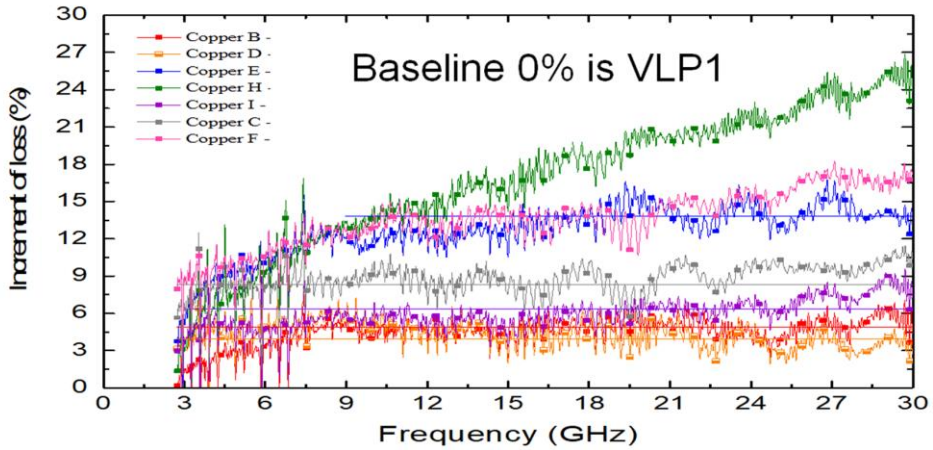
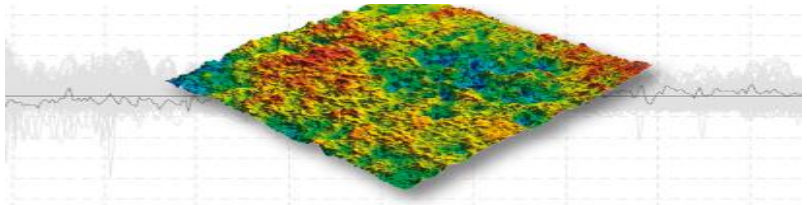


Illustration by courtesy of Isola



Status:

- Of interest to OEM's, EMS providers, PCB fabricators, PCB laminate & copper foil suppliers.
- Chaired by Dupont and Dell
- 13 members & 3 non-members participating
- Passed Concept Gate now at Definition Stage
- Defining scope and drafting SOW
- Contact: steve.payne@inemi.org

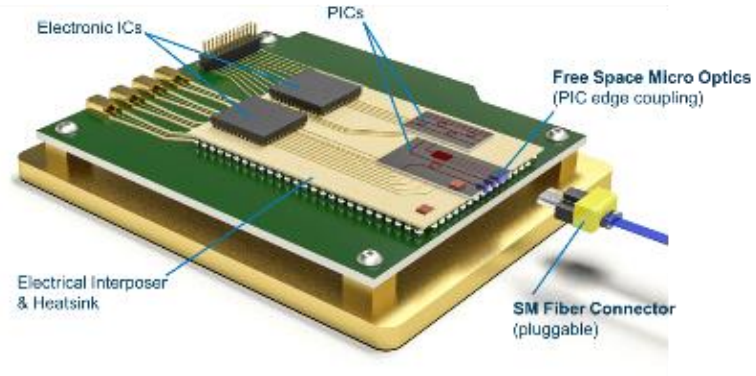
PIC Chip and Micro Optics Demonstrator for Edge Pluggable Free Space Connector - Phase 1

Motivation:

- Singlemode expanded beam interconnects demonstrate optical and mechanical functionality for future system architectures:
- Need to assess the technology benefits and manufacturing issues of using SM expanded-beam connector interfaces in board-level optical interconnect

Objective:

- Build and demonstrate a board-level optical interconnect system in which an expanded-beam optical connector interface will be developed for the chip module
- Develop manufacturing guidelines for PIC module and micro optics



Tyndall Institute

Strategy/Approach:

- Design, assemble and test a PIC module
- Objective: Validate the design for connectors companies – manufacturable open standard
- Timeline: 6-9 mths (depends on chips availability)

Longer term:

- Phase 2: Full demo build with Expanded-beam receptacle & connector for module
- Phase 3: SM Expanded-Beam Connectors for module-waveguide connections, for PCB-embedded waveguide technology

Status:

- Chaired by Tyndall Institute
- 10 orgs involved
- SOW in Review
- Additional participation welcomed
- Working on establishing resource availability and schedule
- Plan Call for participation for April Contact: gomalley@inemi.org

Eco-Design for a Circular Economy -- Learning Series Project

Sustainable Electronics

Motivation:

- Consumer and regulators are driving more awareness and change through the supply chain requiring organizations to implement more eco-design principles for their products
- There are a number of leaders in this area but the majority of organizations lack the knowledge base and training in effectively apply eco-design principles across their product life cycle
- Industry leaders in eco-design sharing their insight can have a significant impact on product manufacturing, maintenance, packaging, branding, and end of life throughout the supply chain

Objective:

- Leverage the eco-design knowledge of leaders to implement circular economy approach
- Identify best practices that have the greatest impact by including a holistic view of the product in society and environment
- Increase awareness and mature the industry's ability to implement/practice eco-design best practices – share information at least with iNEMI membership

Strategy/Approach:

- Identify the current leaders around eco-design in, at least, the ICT industry
- Conduct a series of approximately 1 hour interactive public monthly webinar sessions with 2 experts sharing the best practices and thought process for eco-design that their organizations have implemented
- Publish recorded sessions for review and broader distribution and awareness
- Get real-time feedback on the topics so future sessions can be improved and/or focused
- Potentially partner with other organizations (IZM, IPC, etc) to identify speakers, create and advertise sessions

Outcomes:

- Collect presented best practices for future dissemination and discussion among iNEMI members and/or industry
- Create a "best of" presentation from recorded sessions that captures the top practices of the eco-design leaders
- Based on feedback from members during and after sessions, establish projects and identify member leadership for future Sustainable Electronics efforts (TIG, Roadmaps, projects etc)
- Establish iNEMI as a "go to" resource for industry's eco-design efforts

Status (@definition):

- Chaired by IBM
- Framework for session presentations under review
- SOW in progress;
- Identifying partnership opportunities for webinars
- Identifying potential speakers
- Contact: marks@inemi.org

Electromigration in Low Temperature Solder at Board Level
Board Assembly

Motivation:

- Verify if electromigration would be a potential risk for low temperature soldering (LTS) for the 2nd level interconnect (SLI) solder joints
- Almost all published studies to date on electromigration are for first level interconnect

Objective:

- Determine current density vs resistance increase for a range of solder joint sizes (100 microns to 500 microns)

Priority:

- Near term needs; high industry influence

Strategy/Approach:

- Design appropriate test vehicles which can pass current in both directions through mixed alloy solder joints
- Focus on SLI – BGA solder Joints, both mixed SAC-BiSn and homogenous Bi-Sn
- Microstructural characterization post electromigration

Leadership/Participants:

- Intel, IBM, Nokia, Dell, Indium, Heraeus, Shinko, MacDermid Alpha expressed interest
- Universities can be engaged
- Contact: Haley.Fu@inemi.org

PCB Fiberglass Cloth Characterization for CAF Failure Mitigation
PCB

Motivation:

- CAF (conductive anodic filament) failures are an electrochemical migration process causing short circuits within a PCB. Reduced via hole pitch and low loss resin systems (for 5G and similar applications) have exacerbated the problem which often is only found in the field.
- CAF failures often influence design rules across industry potentially increasing costs.

Objective:

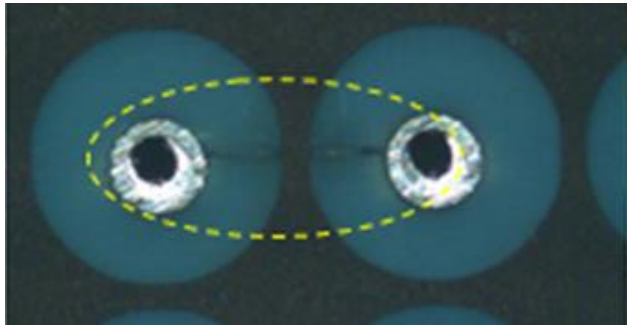
- To characterize effect of glass cloth on reliability of PCB by separating failure mode from effect of low loss resins and copper foil.
- Investigate the effect of fabrication techniques typical for 5G and high frequency designs.

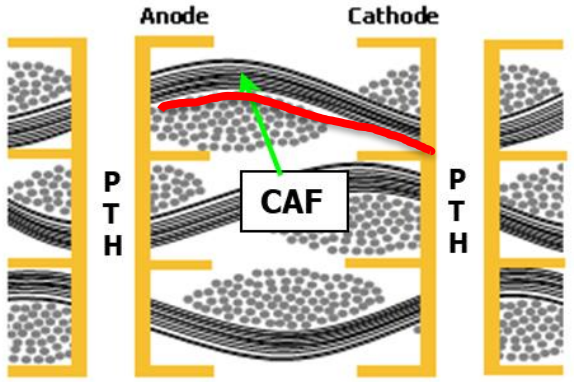
Strategy/Approach:

- Investigate current and recent programs investigating CAF failures to ensure Project is supplementary and complimentary.
- Develop inspection techniques for glass cloth (e.g., air permeability) as a screening test to provide assurance of materials acceptability.

Longer term:

- Best practice guidelines





Illustrations by courtesy of Isola

Status:

- At Concept Stage
- Of interest to OEM's, Tier 1 and EMS providers.
- Meetings ongoing to define scope
- Participation welcome
- Contact Steve.Payne@inemi.org

Reliability Testing of Hybrid PCB for RF applications

Motivation:

- A hybrid multilayer PCB uses dissimilar materials to optimize electrical performance for high-frequency applications whilst reducing costs. A key challenge is predicting PCB reliability and durability for various material combinations.

Objective:

- To develop a predictive comparative simulation tool, to provide guidance for combining different resin systems.

Strategy/Approach:

- Investigate cure kinetics and rheology characterization of a range of laminate resin systems typically considered for high frequency and 5G PCB product.
- Investigate key fabrication processes such as via hole formation and subsequent resin de-smear (chemical and plasma)

Longer term:

- Best practice manufacturing procedures

Multilayer PCB X-section with outer layer Microwave laminate

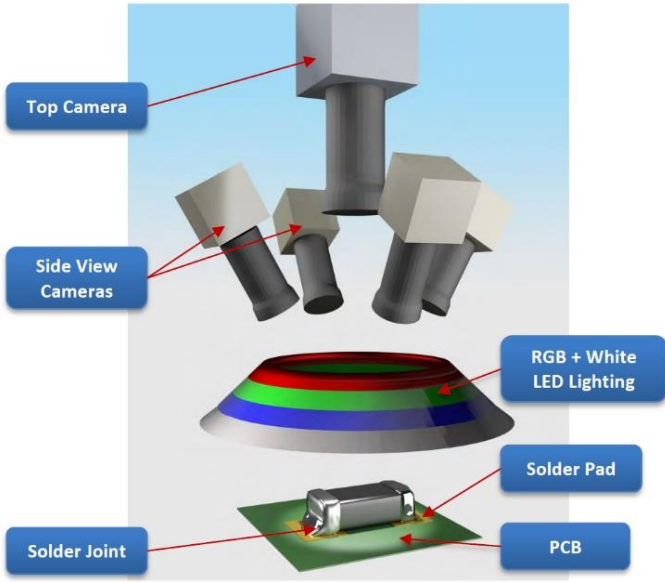
Status:

- Of interest to OEM's - users and designers of PCBs. PCB material suppliers & fabricators
- Draft project scope
- Plan call for interest webinars

Smart AOI Inspection: Demonstrating Capabilities & Identifying Gaps/Opportunities
Board Assembly

Motivation:

- Need to reduce AOI false call and escape rates
- Resulting manual AOI pass/reject is labor intensive
- AOI ramp from design to NPI to volume is iterative and time consuming
- Predictive analytics incorporating AI-based solutions offer significant opportunities with defect identification and judgement; however, accuracy and efficiency needs to be better understood



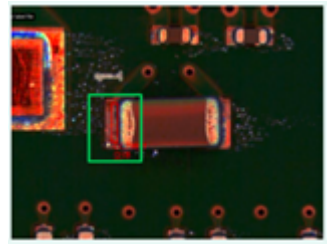
Courtesy of TRI paper

Objective:

- Evaluate existing AOI+AI solutions, identify gaps, recommend best practices, and suggest areas for future development

Strategy/Approach:

- Survey the current of AOI+AI solution landscape
- Initial phase to focus on specific PCBA inspection with test vehicles
- Assess key performance attributes (e.g., accuracy, false call, escape, cycle time, etc.)
- Subsequent phases could expand scope to additional AOI+AI application areas (such as PCB, packages).
- Key participants include: EMS providers, AOI vendors, AI solution providers



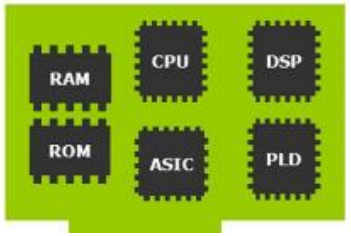
Status:

- Led by IBM the concept is being developed in conjunction with Smart Manufacturing TIG
- Contact: Haley.Fu@inemi.org

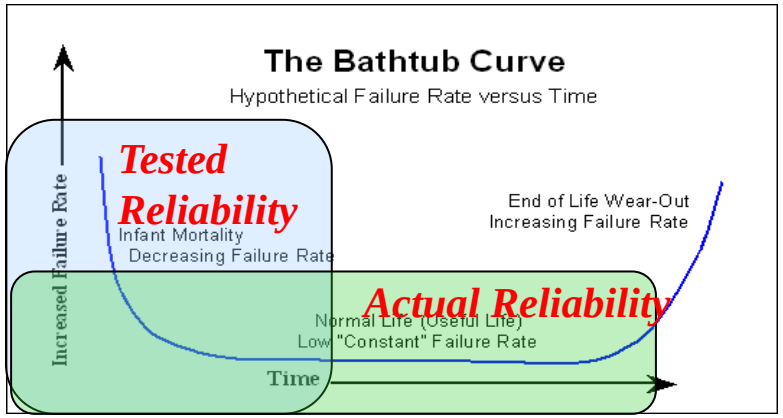
Extended Reliability Assessment for Electronic Components
Sustainable Electronics

Motivation:

- Extended reliability assessment can be used to select products to be refurbished or re-assembled for longer use, reducing consumption of raw materials and processes.
- Enable the use of components beyond shelf life for reduction in waste.
- Limited data for extended reliability assessments: increased lifetime of used parts, qualification process for extended use.
- Lack of standard processes to assess extended reliability of electronic components.



Svstem on Board



Objective:

- From a proof of concept data collection plan, develop a standardized procedure for extended reliability assessment and component classification

Strategy/Approach:

- Identify and classify **new** components by type (application), re-workability and criticality on system.
- Select components (IC, passive or others) and subject to extended reliability. If possible, re-use reliability models to assess reliability extension.
- Select parts in use post 3+ years and subject to reliability to assess further fail rates.

Longer Term:

- Share best practices and experiences across the industry
- Develop standard for understanding or assessing a part long term reliability.

Status:

- Chaired by INTEL, 6 members
- Working on initial draft of SOW
- Conducting a survey of the TIG and TC members on their interest and input to inform SOW development
- Late Q1 potential Launch
- Contact : marks@inemi.org

5G Test Methodology Challenges
5G

Motivation:

- 5G requires development and advancement of new testing methods
- Antenna in package (AiP) devices require a radical change to the existing contact test solutions
- Over The Air (OTA) solutions need to evolve to cost-effective hardware and protocols
- RF Front end modules require new SLT (system level test) concepts due to multitude of bands and carrier aggregation

Objective:

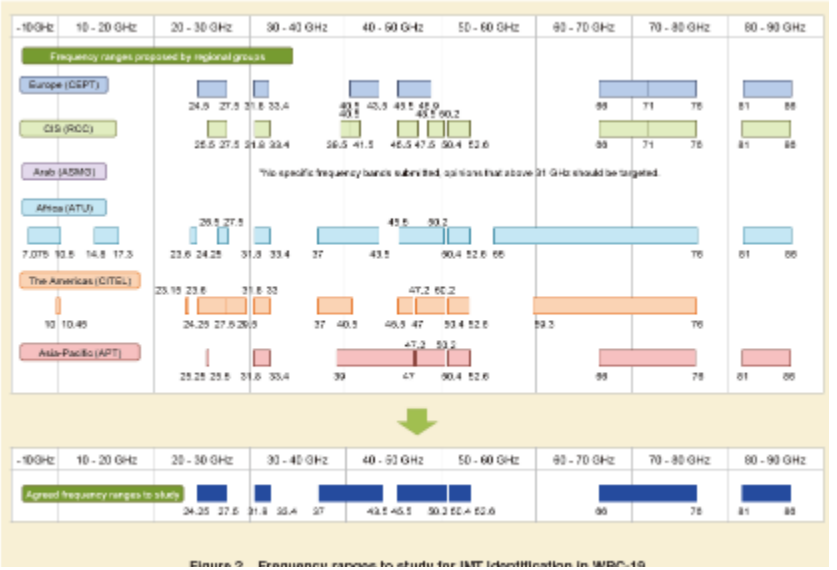
- Need to determine best cost-effective approaches for testing at package/module, board and system level
- Test strategies may be market driven (mobile vs network)

Strategy/Approach:

- Understand and benchmark current status
- Define key gaps and work toward solution

Status:

- Brainstorming sessions underway with small team for project scope development
- To participate contact urmi.ray@inemi.org



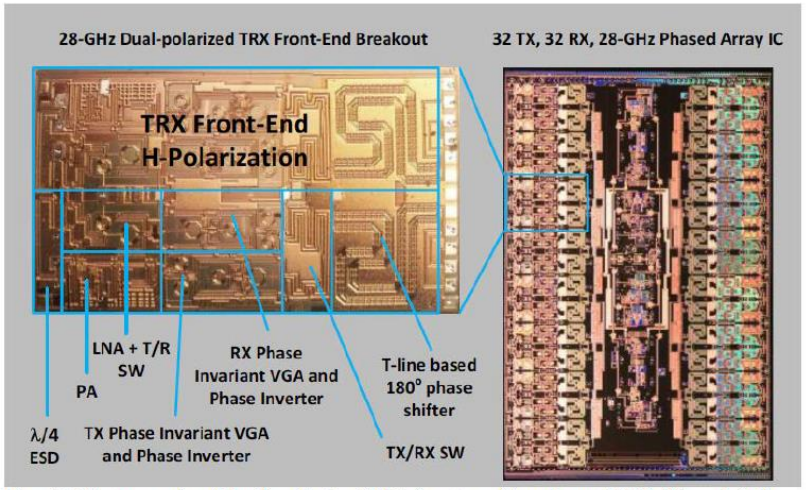


Fig. 7. Photograph of dual-polarized RF front-end breakout IC (left) and full 32-element phased array IC (right)

Solder Joint Quality Requirement of PiP for Through Hole Mounting (THM)
Board Assembly

Motivation:

- Pin-in-Paste Process development can replace wave soldering
- Argument exists on how much fillet needed for THM
- Fillet for PiP mostly appears on the top side instead of secondary side

Objective:

- Process validation with relevant design rules to meet THM fill requirements
- Recommendations to the standard development (IPC A-610 J-STD-001)

Priority:

- Near/mid term needs; High industry influence:

Strategy/Approach:

- Both SAC and low temperature solder to be evaluated
- Leverage some amount of knowledge work done by ODMs

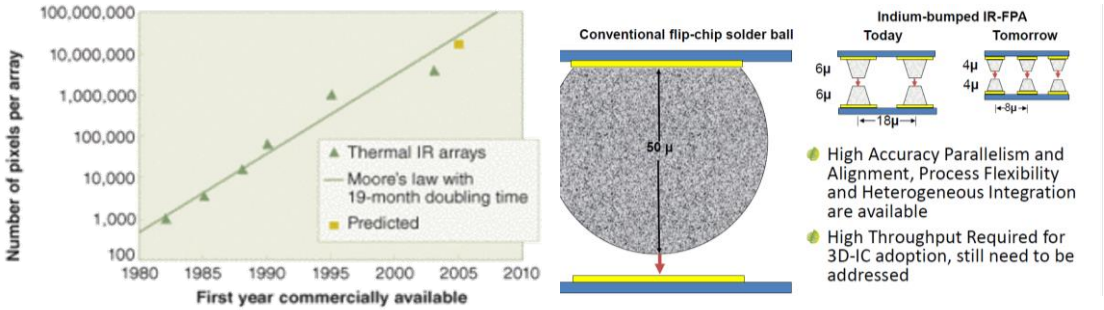
Leadership/Participants:

- Expect leadership from OEM/EMS
- Contact: Haley.Fu@inemi.org

Low Temperature Solders for 1st Level Interconnection
Packaging

Motivation:

- Selection of materials for packaging interconnect is critical.
- The temperature profile required to effect a particular stage should not compromise the integrity or reliability of previous stages,
- The function provided in each stage should not be susceptible to damage by the thermal profiles required by subsequent stages in the manufacture of the package, including testing, and final assembly of the device into the end products.



Objective:

- Provide data-based guidance on the characterization and selection of interconnect materials that can deliver an overall reduction on the process temperature required in the first level construction of IC packages.

Strategy/Approach:

- Research the low temp solder material, soldering technology and applicable products.
- Develop and publish characterization and selection guidelines

Longer Term:

- Recommendations to Standard Body.

Status:

- Concept development led by Indium and IBM
- Packaging TIG workgroup defining concept
- Open to new participants
- Contact Masahiro Tsuriya email: m.tsuriya@inemi.org

Advanced Packaging Test Methodology Optimization
Packaging

Motivation:

- SiP and heterogeneous packages bring complex challenges, in design assembly and test
- Test economics (where and what the test points are), is key gap for SiP

Objective:

- Develop best practices for selective packages

Strategy/Approach:

- Optimization of test infrastructure for best ROI
  - Test insertion choices and cost-benefit analysis
  - Application specific testing (mixed signal, digital etc.)
  - Self testing (BIST, Boundary scan)
  - System level test (SLT)
- Provide guidelines for a common set of test methodologies for customization by individual users

Leadership/Participants:

- Expected Participants: OEM/IDM, fabless semiconductor, foundries, OSATs, test (ATE and instrument) houses

Status:

- Recruiting participants
- Planning WebEx in to follow up on initial roundtable discussions and input.
- Contact:
- urmi.ray@inemi.org

Pad Cratering Mitigation
PCB

Motivation:

- Mitigation of Field Failures due to Mechanically Induced Resin Fracture in Outermost layer of Fiberglass of a PCB
- Presently pad cratering can be difficult to detect during functional testing, especially with small or partial cracking that can cause latent field failures

Objective:

- To develop recommendations to mitigate pad cratering occurrence under Area Array Solder Ball interconnections.

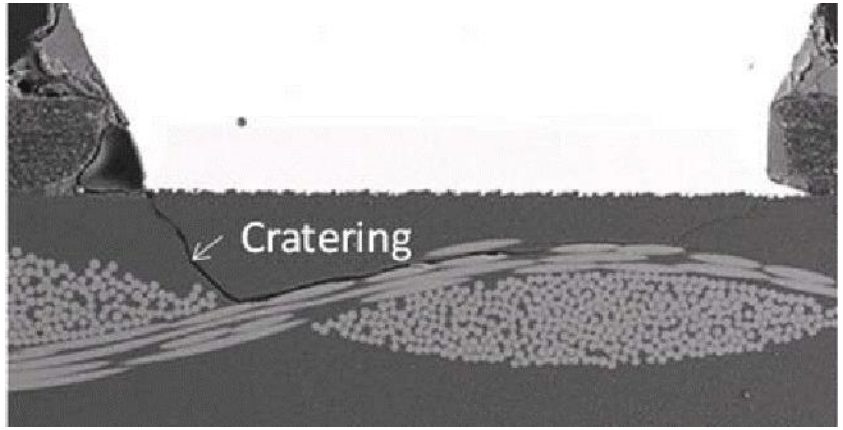
Strategy/Approach:

- Investigate the impact PCB design structure, materials, underfill compound etc. on the propensity to cause pad cratering related to thermal mechanical stress during reflow soldering

Longer term:

- Report to standard bodies

Example of Pad Cratering



Status:

- Of interest to OEM's, Tier 1 and EMS providers.
- Developing project scope
- Participation welcome
- Contact Steve.Payne@inemi.org

PCB Level Interconnect for Co-Packaged Optics Challenges

PCB / Optoelectronics

Motivation:

- To date, introducing Fibre Optics or Optical Waveguides into rigid or flex PCBs has been investigated for 15 years but despite extensive research and numerous papers and patents on the subject it has still not been widely adopted.

Objective:

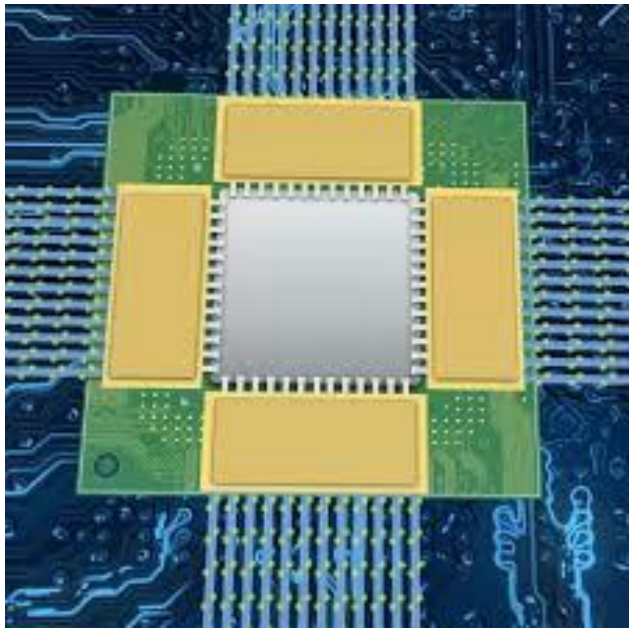
- To investigate and evaluate different technology solutions for dense on-board optical interconnect schemes for co-packaged optics. These may include modern fiber optic flex planes and shuffles, polymer waveguides and planar glass waveguides.

Strategy/Approach:

- Develop PCB level demonstrator. Obtain samples from project members and investigate and evaluate optical performance and manufacturing costs

Longer term:

- Report to industry on manufacturing and cost issues
- Address key gaps to high volume manufacturing



Status:

- Of interest to OEM's, PCB fabricators, and all those involved with photonics integration & co-packaged optics.
- Participation welcomed to define the scope
- Contact: Steve.Payne@inemi.org

iNEMI Contacts:

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